OIPE
FEB 17 2005
PATENT & TRADEMARK OFFICE
JC11

BEST AVAILABLE COPY

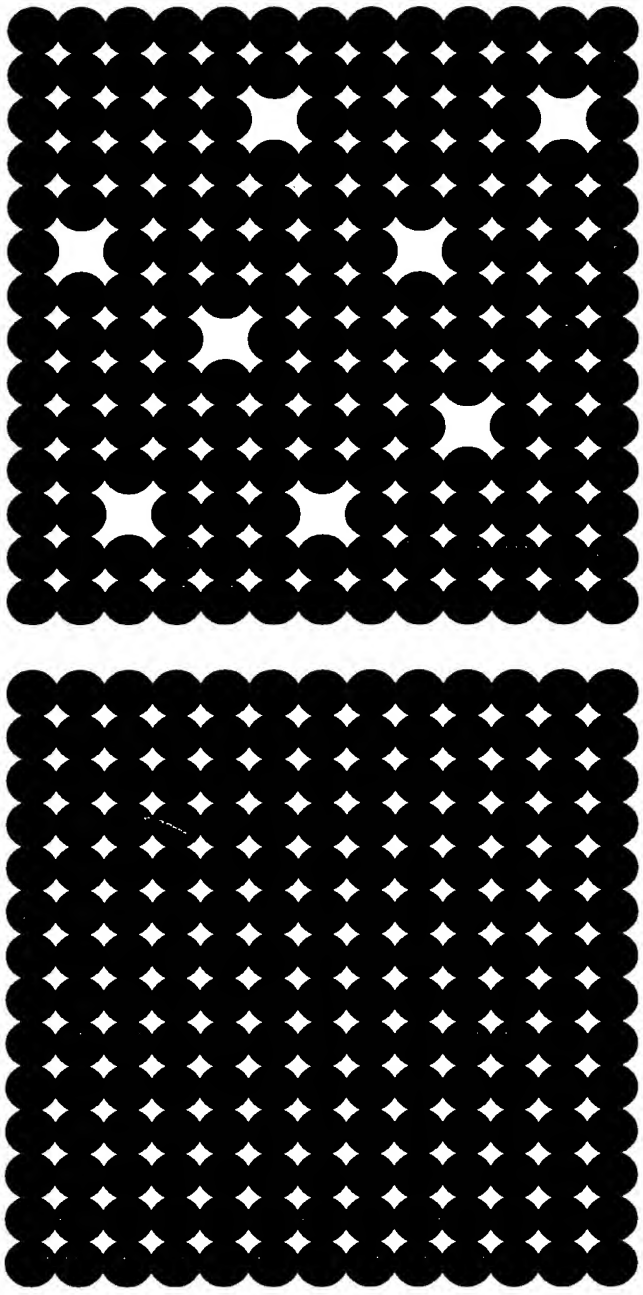

FIG. 1

BEST AVAILABLE COPY

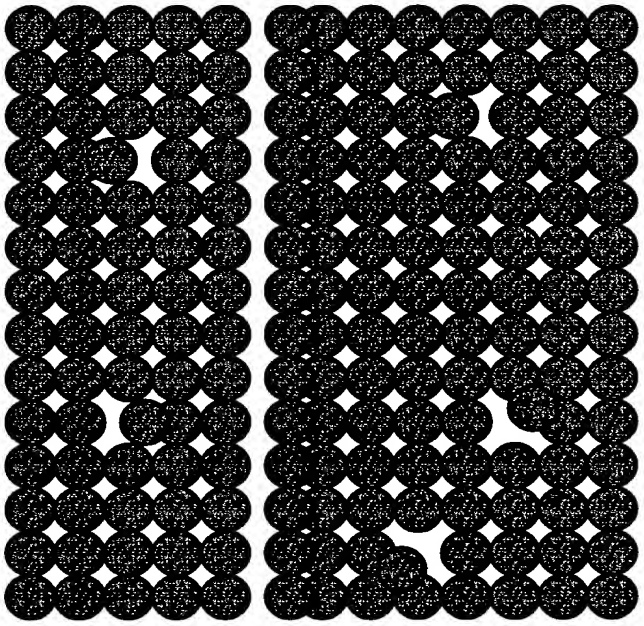

FIG. 2

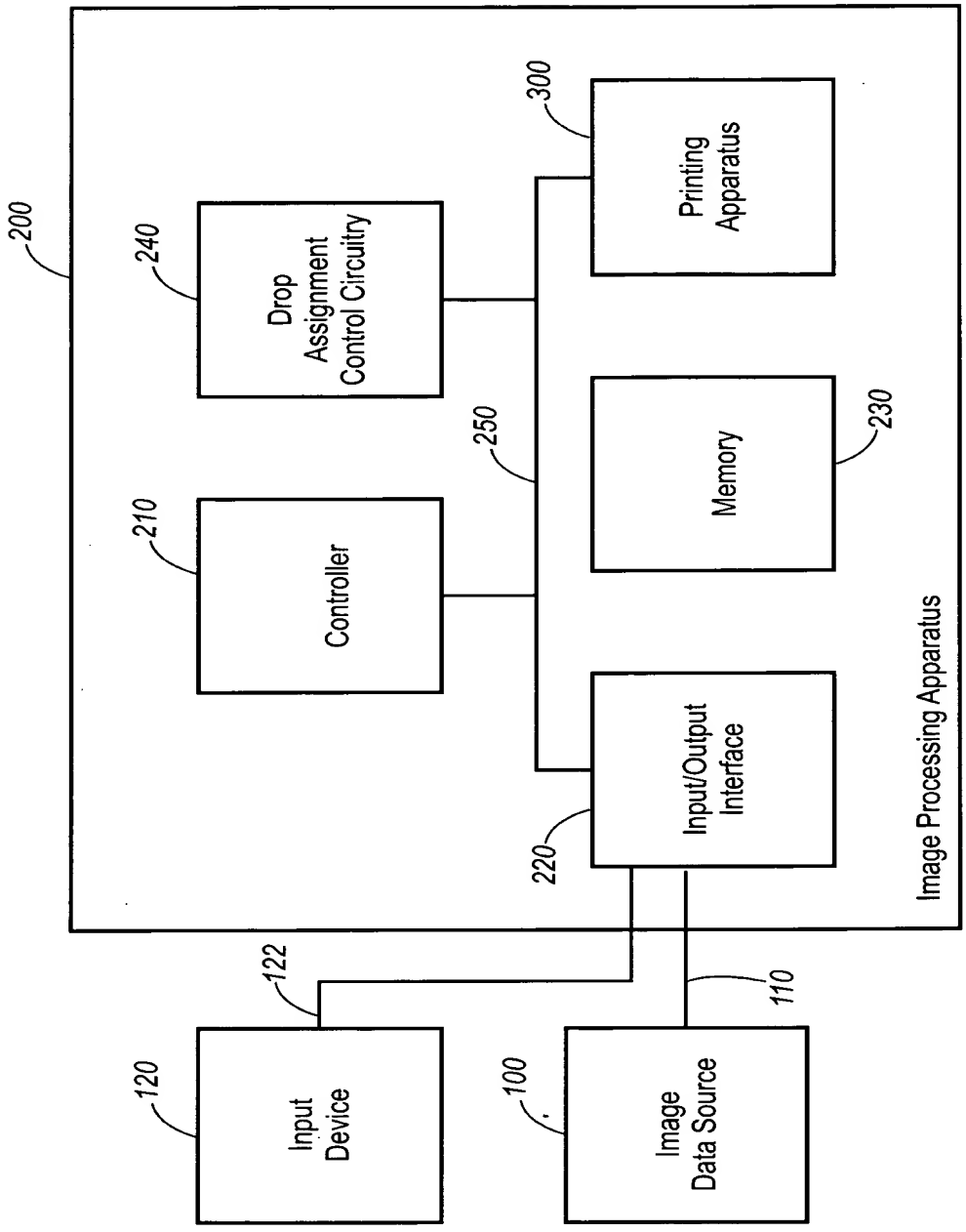
200
Image Processing Apparatus
240
Drop Assignment Control Circuitry
300
Printing Apparatus
250
210
Controller
Memory
230
220
Input/Output Interface
122
110
120
Input Device
100
Image Data Source

FIG. 3

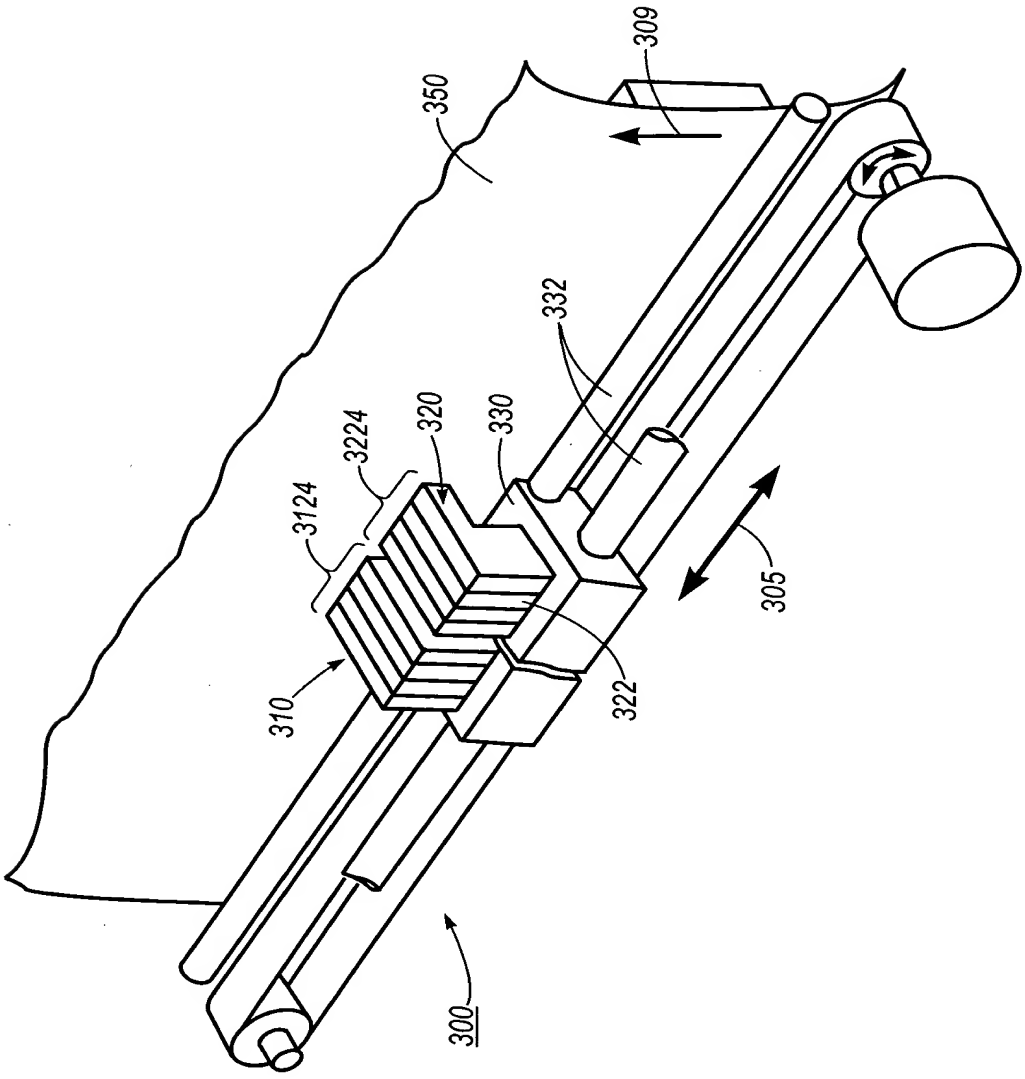

FIG. 4

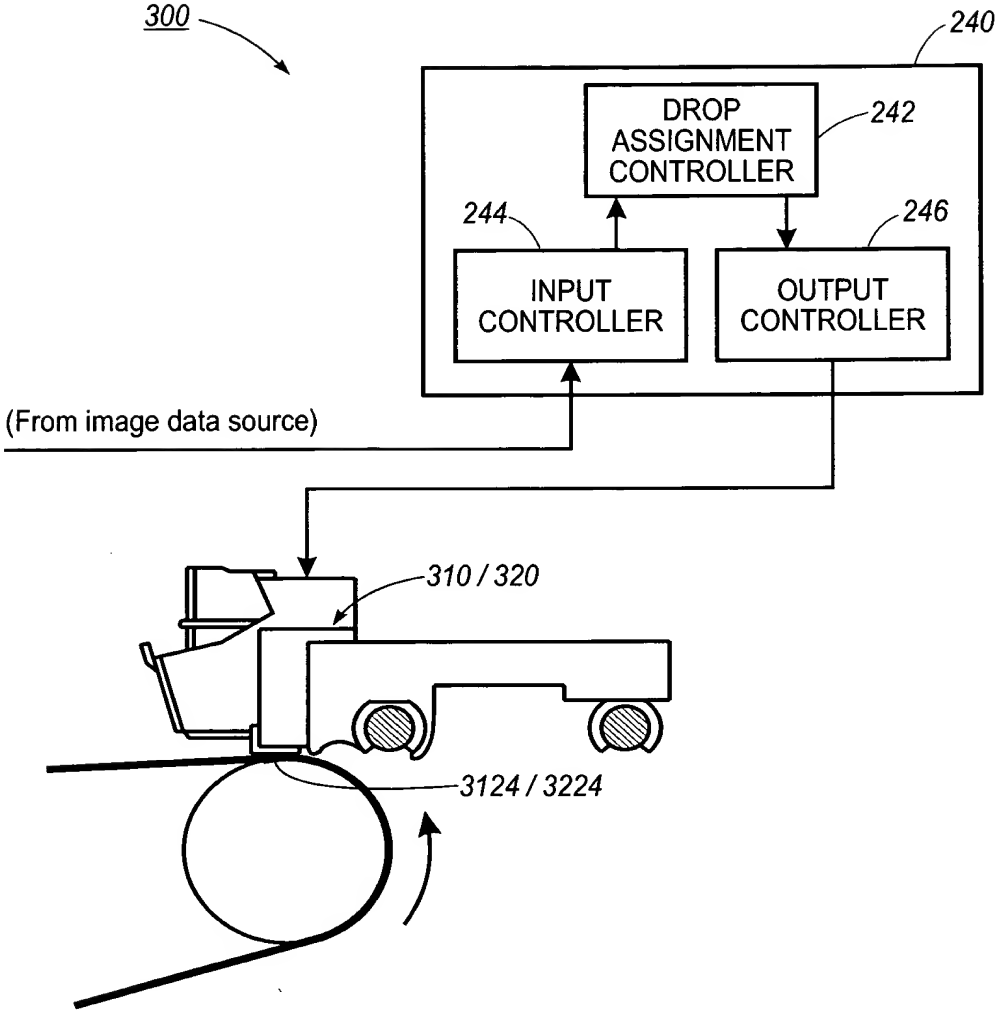
300
240
DROP ASSIGNMENT CONTROLLER
242
244
246
INPUT CONTROLLER
OUTPUT CONTROLLER
(From image data source)
310 / 320
3124 / 3224

FIG. 5

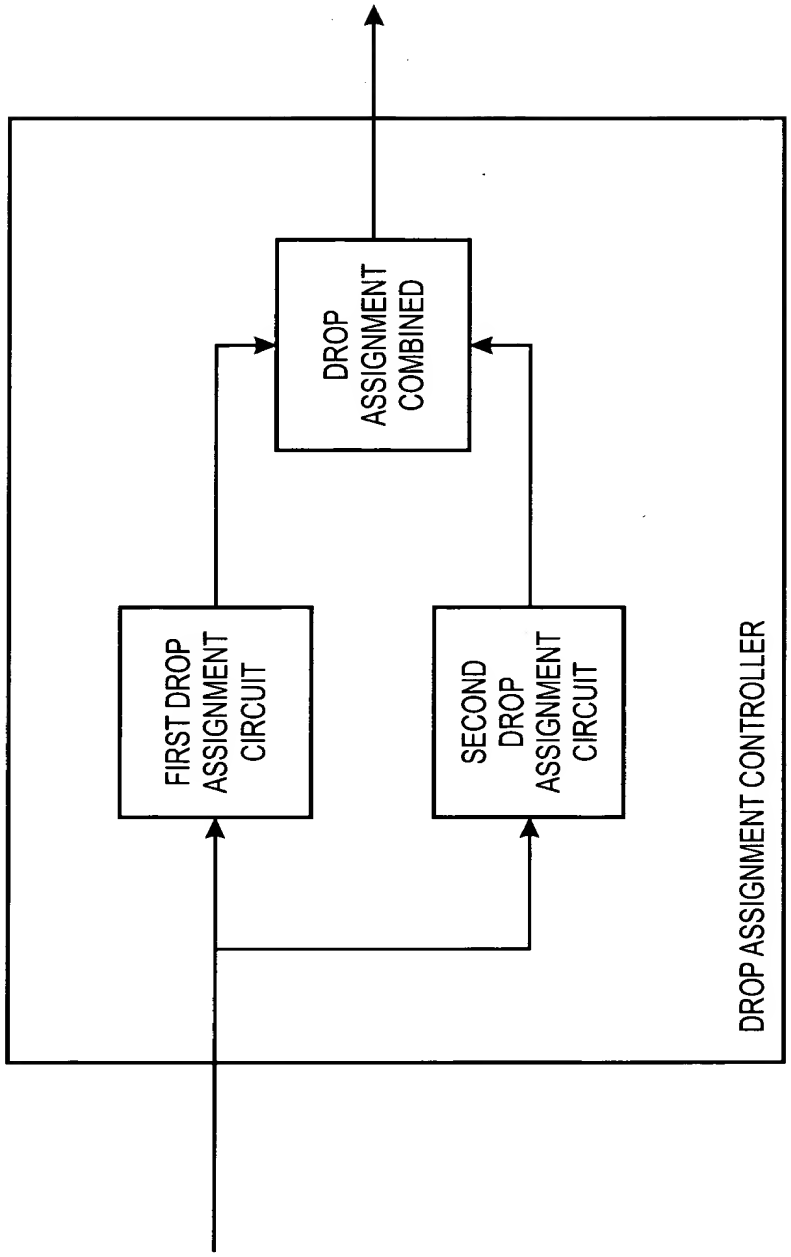
DROP ASSIGNMENT CONTROLLER
FIRST DROP ASSIGNMENT CIRCUIT
SECOND DROP ASSIGNMENT CIRCUIT
DROP ASSIGNMENT COMBINED

FIG. 6

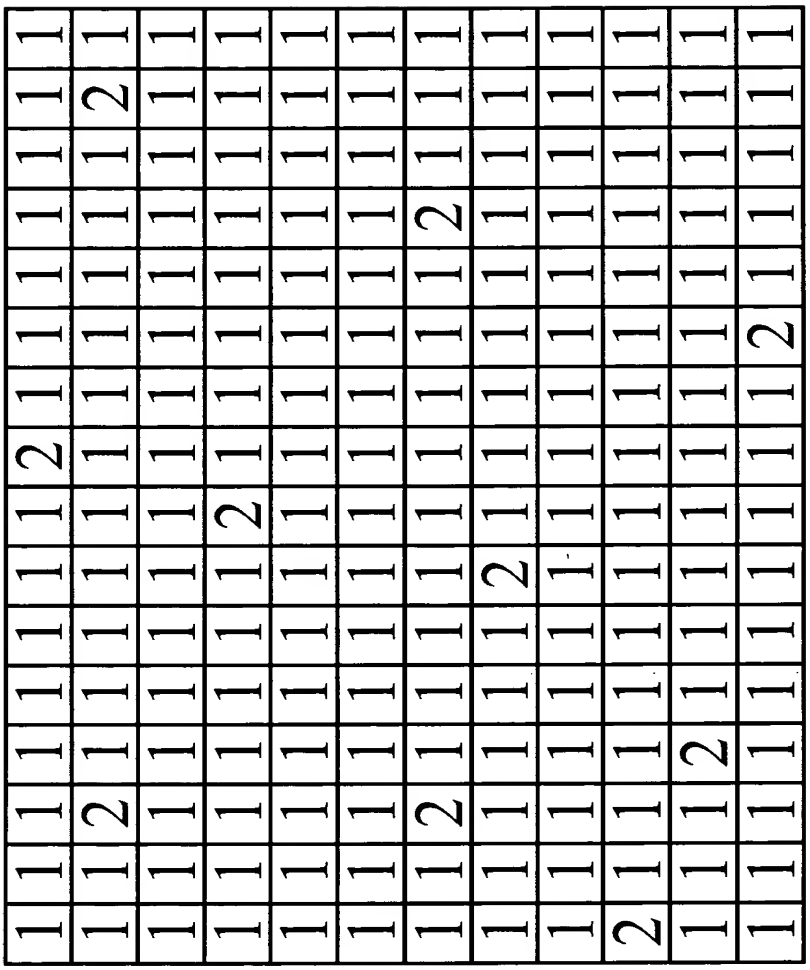
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 2 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 2 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 2 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 2 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 2 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 2 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 2 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 2 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 2 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 2 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 2 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 2 1

FIG. 7

1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	2	1	0	1	1	2	1	1	1	1	1	1	1	1
1	1	1	1	1	2	1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	2	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	2	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

FIG. 8

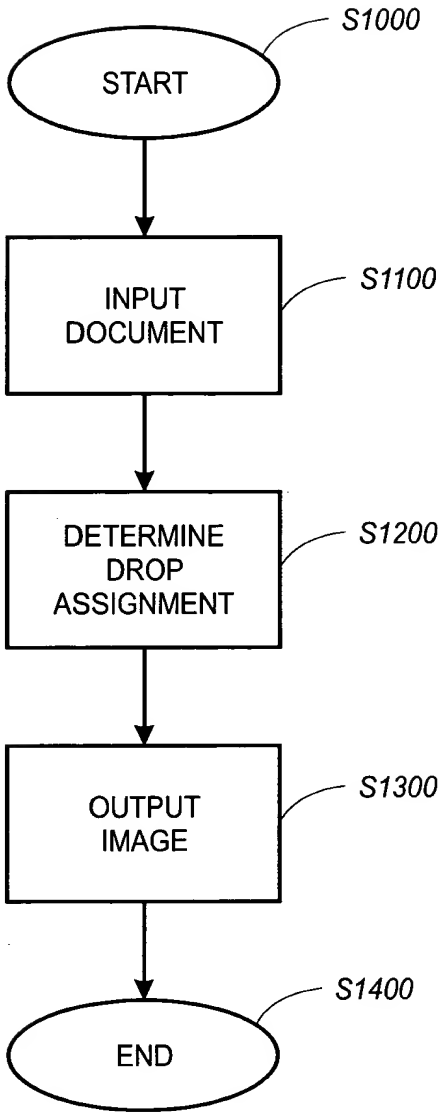
S1000
START
INPUT DOCUMENT
S1100
DETERMINE DROP ASSIGNMENT
S1200
OUTPUT IMAGE
S1300
END
S1400

FIG. 9

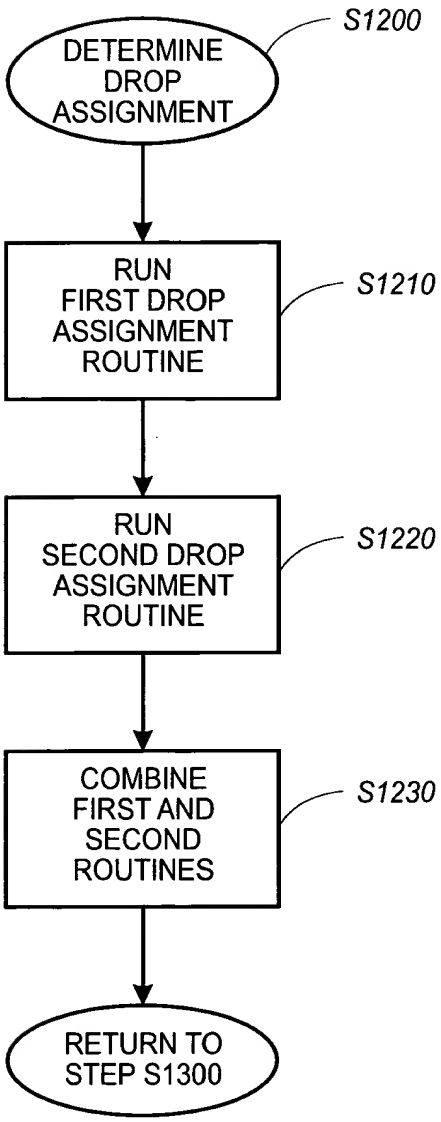
DETERMINE DROP ASSIGNMENT
S1200
RUN FIRST DROP ASSIGNMENT ROUTINE
S1210
RUN SECOND DROP ASSIGNMENT ROUTINE
S1220
COMBINE FIRST AND SECOND ROUTINES
S1230
RETURN TO STEP S1300

FIG. 10